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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,875	LIN, JOHNSON	
	Examiner	Art Unit	
	Gabriel L. Chu	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 6 and 10 are objected to because of the following informalities:

Referring to claim 6, "said second device" has no antecedent basis in claim 1. Claim 6 is understood to depend from, instead, claim 5. Further, "said second frequency" has no antecedent basis. It is understood to refer to "a second frequency".

Referring to claim 10, "said third device" has no antecedent basis in claim 5. Claim 10 is understood to depend from, instead, claim 9. Further, "said third frequency" has no antecedent basis. It is understood to refer to "a third frequency".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 12 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in Paper No. 1 filed 30 March 2001. In that paper, applicant has stated the invention of the present application comprises a series of steps wherein a first device (RAM), a second device (BIOS), and a third device (display adapter) are tested, each resulting in an indication of error, if present (See Applicant's summary and portions of the specification describing figures 5 and 6), and this statement indicates that the invention is different from what is defined in the claim(s) because claim 12

specifically states the BIOS error is detected during the detection of error for the third device. For the purpose of examination, this claim is interpreted, broadly, as a step encompassing both BIOS error and third device error.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5, 7-9, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327435 to Warchol further in view of US 5012514 to Renton and US 5630142 to Crump et al. Referring to claim 1, Warchol discloses a method for identifying a failed device in a computer, said method comprising steps of: providing a memory having a plurality of memory locations containing data values representing a series of computer program instructions for testing a device in said computer (From the abstract, "A processor including a serial port reads processor module diagnostic test instructions from a PROM in a serial line controller through the serial port by way of a serial bus in response to power-up reset instructions."); detecting a first device in said computer to determine whether said first device is failed (From the abstract, "Also, an apparatus and method for indicating module failures in a computer system is provided."); providing a luminescent display which is mounted on the casing of said computer (From the abstract, "A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module.");

and if said first device is detected to be failed, displaying the error on the luminescent display (From the abstract, "Any LED which remains lit indicates the failure of the corresponding module."). Although Wachol does not specifically disclose the memory is a BIOS and detecting an error contained in said memory wherein a predetermined one of said memory locations contains an error detection value based on said data value at the remaining memory locations of said BIOS memory, a BIOS capable of performing a checksum is known in the art. An example of this is shown by Renton, from line 60 of column 3, "As the computer performs its booting actions, the basic input/output system (BIOS) of the computer will scan the locations from C0000H up to E0000H searching for BIOS extension ROMS. The BIOS does this by looking for the flag bytes 55H and AAH. When the BIOS sees these two flag bytes, the next byte is assumed to be the number of 512 byte sectors that the BIOS extension ROM occupies. The BIOS then performs a checksum operation by adding together all of the bytes from the 55H and AAH flag bytes up through the last byte of the last 512 byte sector. The result of this operation must be 00H, in modulo 256. The EPROM programming is performed so that a byte is modified when programming the EPROM such that this checksum will yield the correct result. Once the BIOS has established that the BIOS extension ROM exists and has the correct checksum, the BIOS will perform a far call to the location after the size byte (three bytes after the 55H flag byte). The purpose of this call is to allow the BIOS extension ROM to perform any needed initialization functions that it requires. The extension ROM can then return with a far return, which causes the BIOS to continue its scanning operations for the next BIOS extension ROM." A person of ordinary skill in the

art at the time of the invention would have been motivated to incorporate a BIOS with checksum into a computer system because it performs booting actions and identifies corrupted data. Further, although Warchol does not specifically disclose the luminescent display is a single lumniscent display, blinking said luminescent display ON and OFF at a first frequency if said first device is detected to be failed, using a single element to represent multiple states is known in the art. An example of this is shown by Crump et al., from line 39 of column 4, "Also according to the present invention, the microcontroller controls a light emitting diode (LED) or other suitable visual indicator to provide visual feedback to the user regarding the state of the computer system. Preferably, the power LED is used. When a message has been received and the machine subsequently turns off, the LED is able to flash, thus notifying the user that a message is waiting. The LED can be blinked to indicate the number of messages received while the user was away. A BIOS call allows the various applications to affect the state of the feedback LED by, for example, adding one to the sequence of flashes flashed by the LED." Further, from line 39 of column 23 from Crump et al., "In addition, the LED 23 can be selectively flashed at a particular rate, e.g., every second, by the microcontroller U2 to indicate that the system is in the standby state 152. In addition, the LED 23 can be selectively flashed at a different rate, e.g., every half-second, by the microcontroller U2 to indicate that the system was awakened by a ring or by the alarm and the system is in either the off state or the suspend state. In the alternative, while in the suspend state, the LED 23 can be selectively flashed in groups of flashes by the microcontroller U2 to indicate the number of times the system was powered up by

external events, such as a ring, alarm, etc., and was powered back down by the expiration of the inactivity suspend timer. In this case, the BIOS is provided with one or more functions to allow the OS and application programs to modify the number of times the microcontroller U2 is to flash the LED 23. For example, if the system is awakened by a ring and an incoming facsimile transmission is received, the telecommunications application program can call the particular BIOS function to add one to the number of flashes. Thereafter, the BIOS causes the CPU 40 to write the new flash value to the microcontroller U2, which then causes the LED 23 to flash the commanded number of times." A person of ordinary skill in the art at the time of the invention would have been motivated to use a single LED to display multiple states because, from line 41 of column 4, "to provide visual feedback to the user regarding the state of the computer system" and, further, "Preferably, the power LED is used."

Referring to claims 2 and 7, Warchol in view of Renton and Crump et al. (herein referred to as WRC) discloses the step of detecting said first or second device in said computer comprises a step of identifying a type and an identification of said first or second device in said computer by means of said BIOS memory (From line 19 of column 3 of Warchol, "According to a further aspect of the invention, an apparatus and method for indicating module failures in a computer system is provided. Broadly stated, this aspect of the invention operates in a computer system comprising one or more CPU modules, an I/O module, and one or more memory modules. A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module. Any LED which remains lit indicates the failure of

the corresponding module.").

Referring to claims 3 and 8, WRC discloses the step of detecting said first or second device in said computer comprises a step of: analyzing the data values and said error detection value at said predetermined memory location in said BIOS memory to detect whether an error is contained within said BIOS memory (From line 60 of column 3 of Renton, "As the computer performs its booting actions, the basic input/output system (BIOS) of the computer will scan the locations from C0000H up to E0000H searching for BIOS extension ROMS. The BIOS does this by looking for the flag bytes 55H and AAH. When the BIOS sees these two flag bytes, the next byte is assumed to be the number of 512 byte sectors that the BIOS extension ROM occupies. The BIOS then performs a checksum operation by adding together all of the bytes from the 55H and AAH flag bytes up through the last byte of the last 512 byte sector. The result of this operation must be 00H, in modulo 256. The EPROM programming is performed so that a byte is modified when programming the EPROM such that this checksum will yield the correct result. Once the BIOS has established that the BIOS extension ROM exists and has the correct checksum, the BIOS will perform a far call to the location after the size byte (three bytes after the 55H flag byte). The purpose of this call is to allow the BIOS extension ROM to perform any needed initialization functions that it requires. The extension ROM can then return with a far return, which causes the BIOS to continue its scanning operations for the next BIOS extension ROM.").

Referring to claim 5, WRC discloses detecting a second device in said computer to determine whether said second device is failed (From the abstract of Warchol, "Also,

an apparatus and method for indicating module failures in a computer system is provided. A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module."); and if said second device is detected to be failed, blinking said single luminescent display ON and OFF at a second frequency different from said first frequency (From line 39 of column 23 from Crump et al., "In addition, the LED 23 can be selectively flashed at a particular rate, e.g., every second, by the microcontroller U2 to indicate that the system is in the standby state 152. In addition, the LED 23 can be selectively flashed at a different rate, e.g., every half-second, by the microcontroller U2 to indicate that the system was awakened by a ring or by the alarm and the system is in either the off state or the suspend state. In the alternative, while in the suspend state, the LED 23 can be selectively flashed in groups of flashes by the microcontroller U2 to indicate the number of times the system was powered up by external events, such as a ring, alarm, etc., and was powered back down by the expiration of the inactivity suspend timer. In this case, the BIOS is provided with one or more functions to allow the OS and application programs to modify the number of times the microcontroller U2 is to flash the LED 23. For example, if the system is awakened by a ring and an incoming facsimile transmission is received, the telecommunications application program can call the particular BIOS function to add one to the number of flashes. Thereafter, the BIOS causes the CPU 40 to write the new flash value to the microcontroller U2, which then causes the LED 23 to flash the commanded number of times.").

Referring to claim 9, WRC discloses detecting a third device in said computer to

determine whether said third device is failed (From the abstract of Warchol, "Also, an apparatus and method for indicating module failures in a computer system is provided. A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module."); and if said third device is detected to be failed, blinking said single luminescent display ON and OFF at a third frequency different from said first frequency and said second frequency (From line 39 of column 23 from Crump et al., "In addition, the LED 23 can be selectively flashed at a particular rate, e.g., every second, by the microcontroller U2 to indicate that the system is in the standby state 152. In addition, the LED 23 can be selectively flashed at a different rate, e.g., every half-second, by the microcontroller U2 to indicate that the system was awakened by a ring or by the alarm and the system is in either the off state or the suspend state. In the alternative, while in the suspend state, the LED 23 can be selectively flashed in groups of flashes by the microcontroller U2 to indicate the number of times the system was powered up by external events, such as a ring, alarm, etc., and was powered back down by the expiration of the inactivity suspend timer. In this case, the BIOS is provided with one or more functions to allow the OS and application programs to modify the number of times the microcontroller U2 is to flash the LED 23. For example, if the system is awakened by a ring and an incoming facsimile transmission is received, the telecommunications application program can call the particular BIOS function to add one to the number of flashes. Thereafter, the BIOS causes the CPU 40 to write the new flash value to the microcontroller U2, which then causes the LED 23 to flash the commanded number of times." Wherein Warchol

teaches a different indication for each module and Crump et al. teaches a different frequency for each state.).

Referring to claim 13, WRC discloses said error detection value at said predetermined memory location in said BIOS memory contains a checksum value (From line 60 of column 3 of Renton, with emphasis, "As the computer performs its booting actions, the basic input/output system (BIOS) of the computer will scan the locations from C0000H up to E0000H searching for BIOS extension ROMS. The BIOS does this by looking for the flag bytes 55H and AAH. When the BIOS sees these two flag bytes, the next byte is assumed to be the number of 512 byte sectors that the BIOS extension ROM occupies. The BIOS then performs a **checksum** operation by adding together all of the bytes from the 55H and AAH flag bytes up through the last byte of the last 512 byte sector. The result of this operation must be 00H, in modulo 256. The EPROM programming is performed so that a byte is modified when programming the EPROM such that this checksum will yield the correct result. Once the BIOS has established that the BIOS extension ROM exists and has the correct checksum, the BIOS will perform a far call to the location after the size byte (three bytes after the 55H flag byte). The purpose of this call is to allow the BIOS extension ROM to perform any needed initialization functions that it requires. The extension ROM can then return with a far return, which causes the BIOS to continue its scanning operations for the next BIOS extension ROM.").

6. Claims 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327435 to Warchol further in view of US 5630142 to Crump et al. Referring to

claim 14, Warchol discloses a device for displaying a message indicative of a failed device in a computer, comprising: a luminescent display which is mounted on the casing of said computer (From the abstract of Warchol, "A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module."); a memory having a plurality of memory locations containing data values representing a series of computer program instructions for testing a hardware device in said computer, and sending a control signal according to the result of testing said hardware device (From the abstract of Warchol, "A processor including a serial port reads processor module diagnostic test instructions from a PROM in a serial line controller through the serial port by way of a serial bus in response to power-up reset instructions." Further, from line 29 of column 3 of Warchol, "More particularly, power-up diagnostics are executed by an installed CPU. System testing proceeds by turning on the LEDs corresponding to the CPU modules and turning off the LEDs corresponding to all other modules in response to a hardware reset. Diagnostics then proceed by testing one CPU module, and testing a 2nd CPU module if it is installed; turning off the LED corresponding to the one CPU module if the testing of the one CPU module detects no failures; testing for the presence of the 2nd CPU module; turning off the LED corresponding to the 2nd CPU module if it is found to be not present; turning on the LED corresponding to the I/O module; testing for bus access to the I/O module from the Ist CPU module; turning off the LED corresponding to the I/O module if the testing for bus access detects no failures; turning on the LEDs corresponding to the installed memory modules; and, for each memory module that is installed, testing the memory

module, and turning off the LED if the testing of the memory module detects no failures."); and a decoding element receiving said control signal and outputs a driving signal to enable said luminescent display to display said control signal received thereof (From line 9 of column 7, "Each LED corresponds to a particular one of the modules 14, and is lit by the processor 50 of primary CPU module 24 by way of the serial control bus 46 to indicated a failure of the corresponding module."). Although Warchol does not specifically disclose the memory is a BIOS memory and the luminescent display is a single luminescent display and is operable to blink at multiple frequencies, using a single element to represent multiple states is known in the art. An example of this is shown by Crump et al., from line 39 of column 4 (with emphasis), "Also according to the present invention, the microcontroller controls a light emitting diode (LED) or other suitable visual indicator to provide visual feedback to the user regarding the state of the computer system. Preferably, the power LED is used. When a message has been received and the machine subsequently turns off, the LED is able to flash, thus notifying the user that a message is waiting. The LED can be blinked to indicate the number of messages received while the user was away. A **BIOS** call allows the various applications to affect the state of the feedback LED by, for example, adding one to the sequence of flashes flashed by the LED." Further, from line 39 of column 23 from Crump et al., "In addition, the LED 23 can be selectively flashed at a particular rate, e.g., every second, by the microcontroller U2 to indicate that the system is in the standby state 152. In addition, the LED 23 can be selectively flashed at a different rate, e.g., every half-second, by the microcontroller U2 to indicate that the system was

awakened by a ring or by the alarm and the system is in either the off state or the suspend state. In the alternative, while in the suspend state, the LED 23 can be selectively flashed in groups of flashes by the microcontroller U2 to indicate the number of times the system was powered up by external events, such as a ring, alarm, etc., and was powered back down by the expiration of the inactivity suspend timer. In this case, the **BIOS** is provided with one or more functions to allow the OS and application programs to modify the number of times the microcontroller U2 is to flash the LED 23. For example, if the system is awakened by a ring and an incoming facsimile transmission is received, the telecommunications application program can call the particular **BIOS** function to add one to the number of flashes. Thereafter, the **BIOS** causes the CPU 40 to write the new flash value to the microcontroller U2, which then causes the LED 23 to flash the commanded number of times." A person of ordinary skill in the art at the time of the invention would have been motivated to use a single LED to display multiple states because, from line 41 of column 4 of Crump et al., "to provide visual feedback to the user regarding the state of the computer system" and, further, "Preferably, the power LED is used."

Referring to claim 15, Warchol in view of Crump et al. discloses said single luminescent display comprises a light-emitting diode mounted on the casing of said computer provided for indicating the power status of said computer (From line 41 of column 4 of Crump et al., "to provide visual feedback to the user regarding the state of the computer system" and, further, "Preferably, the power LED is used.").

Referring to claim 16, Warchol in view of Crump et al. discloses a serial interface

provided for communication between said BIOS memory and said hardware device (From the abstract of Warchol, "A processor including a serial port reads processor module diagnostic test instructions from a PROM in a serial line controller through the serial port by way of a serial bus in response to power-up reset instructions.").

Referring to claim 17, Warchol in view of Crump et al. discloses said serial interface comprises a system management bus interface (From the abstract of Warchol, "A processor including a serial port reads processor module diagnostic test instructions from a PROM in a serial line controller through the serial port by way of a serial bus in response to power-up reset instructions.").

Referring to claim 18, Warchol in view of Crump et al. discloses said decoding element includes an input/output port for transmitting said driving signal to said single luminescent display (From the abstract of Warchol, "A processor including a serial port reads processor module diagnostic test instructions from a PROM in a serial line controller through the serial port by way of a serial bus in response to power-up reset instructions." Further, from line 29 of column 3 of Warchol, "More particularly, power-up diagnostics are executed by an installed CPU. System testing proceeds by turning on the LEDs corresponding to the CPU modules and turning off the LEDs corresponding to all other modules in response to a hardware reset. Diagnostics then proceed by testing one CPU module, and testing a 2nd CPU module if it is installed; turning off the LED corresponding to the one CPU module if the testing of the one CPU module detects no failures; testing for the presence of the 2nd CPU module; turning off the LED corresponding to the 2nd CPU module if it is found to be not present; turning on the

LED corresponding to the I/O module; testing for bus access to the I/O module from the Ist CPU module; turning off the LED corresponding to the I/O module if the testing for bus access detects no failures; turning on the LEDs corresponding to the installed memory modules; and, for each memory module that is installed, testing the memory module, and turning off the LED if the testing of the memory module detects no failures.").

Referring to claim 19, Warchol in view of Crump et al. discloses said decoding element comprises a bridge chip (From figure 2 of Warchol, CPU1 is shown between the Power Subsystem 44 and a "Cobra System Bus" 38. Further, from line 66 of column 10, "The computer then writes data to the non-volatile CMOS memory 96 indicating that the system was suspended. Lastly, the CPU 40 commands the microcontroller U2 to cause the power supply 17 to stop providing regulated power to the system through the .+-.5 VDC and .+-.12 VDC lines. The computer system 10 is now powered down with the entire state of the computer safely saved to the fixed disk storage device 31.").

7. Claims 4, 6, and 10-12 rejected under 35 U.S.C. 103(a) as being unpatentable over WRC as applied to claims 1, 5, and 9 above, and further in view of "How a Computer Wakes Up" by White. Referring to claim 4, WRC discloses providing a sound playing device; and if a device is detected to be failed, driving said sound playing device to beep at said first frequency (From line 63 of column 51 of Crump et al., "The Fatal Suspend Error Routine is found at tasks 652 through 664 and is called at 638 if code with an improper privilege level attempts to save the state of the CPU. First, the Failsafe Timer is RESET, at 654. Then the speaker beeps a number of times at an

audible frequency, e.g., three times at 886 Hz for 0.25 seconds, with 1/6th of a second between beeps, at task 656. The three beeps alerts the user that the attempted suspend did not take place. After beeping, the Failsafe Timer is RESET again at 658 to give the user a consistent 15 to 18 seconds before the Failsafe Timer expires, shutting off the power supply 17."). Although Warchol in view of Renton and Crump et al. do not specifically say this beep is performed in response to the failure of the first device, beeping in response to an error is notoriously well known in the art. An example of this is shown by White, from paragraph 4 of page17, "When the POST detects an error from the display, memory, keyboard, or other basic components, it produces an error warning in the form of a message on your display and – in case your display is part of the problem – in the form of a series of beeps." A person of ordinary skill in the art at the time of the invention would have been motivated to provide sound in addition to visual indication means because, from White, "in case your display is part of the problem".

Referring to claims 6 and 10, WRC discloses indicating a second or third failure through a single indicating means (Indicating errors on LED's as disclosed by Warchol in view of indicating errors on a single LED as disclosed by Crump et al.). Although WRC do not specifically disclose if said second or third device is detected to contain an error, driving said sound playing device to beep at a second or third frequency, playing a sound to indicate the problem, in addition to a display indicating the problem, is known in the art. An example of this is shown by White, from paragraph 4 of page17, "When the POST detects an error from the display, memory, keyboard, or other basic components, it produces an error warning in the form of a message on your display and

– in case your display is part of the problem – in the form of a series of beeps. Usually neither the beeps nor the onscreen message is specific enough to tell you exactly what is wrong. All they're intended to do is to point you in the general direction of the component that has a problem." A person of ordinary skill in the art at the time of the invention would have been motivated to provide sound in addition to visual indication means because, from White, "in case your display is part of the problem".

Referring to claim 11, WRC discloses the step of detecting said third device in said computer comprises a step of identifying a type and an identification of said third device in said computer by means of said BIOS memory (From line 19 of column 3 of Warchol, "According to a further aspect of the invention, an apparatus and method for indicating module failures in a computer system is provided. Broadly stated, this aspect of the invention operates in a computer system comprising one or more CPU modules, an I/O module, and one or more memory modules. A console panel is provided in the computer system comprising LED's visible to the user, each LED corresponding to a particular module. Any LED which remains lit indicates the failure of the corresponding module.").

Referring to claim 12, the step of detecting said third device in said computer comprises a step of: analyzing the data values and said error detection value at said predetermined memory location in said BIOS memory to detect whether an error is contained within said BIOS memory (From line 60 of column 3 of Renton, "As the computer performs its booting actions, the basic input/output system (BIOS) of the computer will scan the locations from C0000H up to E0000H searching for BIOS

extension ROMS. The BIOS does this by looking for the flag bytes 55H and AAH. When the BIOS sees these two flag bytes, the next byte is assumed to be the number of 512 byte sectors that the BIOS extension ROM occupies. The BIOS then performs a checksum operation by adding together all of the bytes from the 55H and AAH flag bytes up through the last byte of the last 512 byte sector. The result of this operation must be 00H, in modulo 256. The EPROM programming is performed so that a byte is modified when programming the EPROM such that this checksum will yield the correct result. Once the BIOS has established that the BIOS extension ROM exists and has the correct checksum, the BIOS will perform a far call to the location after the size byte (three bytes after the 55H flag byte). The purpose of this call is to allow the BIOS extension ROM to perform any needed initialization functions that it requires. The extension ROM can then return with a far return, which causes the BIOS to continue its scanning operations for the next BIOS extension ROM.").

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327435 to Warchol in view of US 5630142 as applied to claim 14 above, and further in view of "How a Computer Wakes Up" by White. Referring to claim 20, Warchol in view of Crump et al. discloses providing a sound playing device, and if a device is detected to be failed, driving said sound playing device to beep at said first frequency (From line 63 of column 51 of Crump et al., "The Fatal Suspend Error Routine is found at tasks 652 through 664 and is called at 638 if code with an improper privilege level attempts to save the state of the CPU. First, the Failsafe Timer is RESET, at 654. Then the speaker beeps a number of times at an audible frequency, e.g., three times at 886 Hz

for 0.25 seconds, with 1/6th of a second between beeps, at task 656. The three beeps alerts the user that the attempted suspend did not take place. After beeping, the Failsafe Timer is RESET again at 658 to give the user a consistent 15 to 18 seconds before the Failsafe Timer expires, shutting off the power supply 17."). Although Warchol in view of Crump et al. do not specifically disclose this sound playing device is drivable to beep at a frequency associated with said control signal received thereof, beeping in response to an error is notoriously well known in the art. An example of this is shown by White, from paragraph 4 of page17, "When the POST detects an error from the display, memory, keyboard, or other basic components, it produces an error warning in the form of a message on your display and – in case your display is part of the problem – in the form of a series of beeps." A person of ordinary skill in the art at the time of the invention would have been motivated to provide sound in addition to visual indication means because, from White, "in case your display is part of the problem".

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 4633469 to Kishi et al.

US 5018143 to Platteter et al.

US 5644707 to Chen

US 5815706 to Stewart et al.

US 6173320 to Cunningham

US 6234111 to Ulman et al.

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US 6601164 to Robertson

US 2002/0032885 to Dai

"MS-6309LE5" by MSI

"D-Bracket" by MSI

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

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